CLAIMS:

1. A semiconductor memory device comprising;

a memory portion which allows data to be rewritten,

an internal circuit having a plurality of operation modes designated by the function signal and deciding data to be offered to said memory portion in each operation mode,

an address input terminal, and

a function setting circuit in which the input signal to be taken thereinto is fed via said address input terminal to form said function signal in accordance with said input signal.

2. A semiconductor memory device as defined in Claim 1, wherein said device comprises a timing control circuit which receives a substantial chip selection signal and a first control signal and when said chip selection signal and said control signal are altered by the predetermined combination, forms a first timing signal, said function setting circuit taking in the input signal in accordance with said first timing signal.

3. A semiconductor memory device as defined in Claim 2, wherein said function setting circuit has a hold means for maintaining the level of said function

signal until said first timing signal is again generated.

4. A semiconductor memory device as defined in Claim 2, wherein it comprises an address buffer the input terminal of which is coupled to said address input terminal, the input signal being fed via said address buffer to said function setting circuit.

5. A semiconductor memory device as defined in Claim 4, wherein said address buffer comprises an address buffer for receiving the row address signal and the column address signal which are fed to said address input terminal in accordance with the time sharing system and said chip selection signal comprises the row address strobe signal, and said first control signal is composed of the column address strobe signal and the write enable signal.

6. A semiconductor memory device as defined in Claim 5, wherein said memory portion comprises a dynamic random access memory.

7. A semiconductor memory device as defined in Claim 6, wherein it comprises further a refresh control circuit for forming at least the refresh address strobe signal for said memory portion and said timing control circuit makes the refresh operation effective by said refreshing control circuit in response to the

column address strobe signal being set to the active level when said row address strobe signal is set to the inactive level and the timing signal is formed so that the input operation of said function setting circuit may be made effective in response to the status wherein, said row address strobe signal and the column address strobe signal are respectively set to the inactive and active levels, while the write enable signal is set too the active level.

8. A semiconductor memory device as defined in Claim 7, wherein said internal circuit comprises an operation circuit whose operation mode is designated by the function signal fed from said function setting circuit, while forming data to be offered to said memory portion in accordance with the input data and the data to be read out from said memory portion.

9. A semiconductor memory device comprising;

a memory portion which allows data to be re-written,

an operation circuit for forming the operation data to be written in said memory portion, receiving the input data and the data to be read out from said memory portion,

a function circuit, and

a bypass circuit the operation of which is

controlled by the control signal fed from said function setting circuit and which, in the operated state, feeds said input data directly to said memory portion.

10. A semiconductor memory device a defined in Claim 9, wherein said operation circuit has a plurality of operation modes and said function setting circuit outputs the operation control signal for controlling said operation mode.

11. A semiconductor memory device as defined in Claim 10, wherein it comprises further a timing control circuit the operation of which is controlled by a plurality of external control signals and when said plurality of external control signals are set to the predetermined state, form the control signal for setting said function setting circuit to the state of input operation, said function setting circuit having a hold means for maintaining said operation control signal and said control signal for said bypass circuit after said state of input operation.

12. A semiconductor memory device as defined in Claim 11, wherein it has further an address input terminal and a coupling means for coupling said address input terminal and the input terminal of said function setting circuit.

a1 13. A semiconductor memory device as defined in Claim 12, wherein said coupling means comprises a column address buffer.

Add A3

Add B1

Add C2